What is claimed is:

1. A CMOS operational amplifier comprising:

an amplifying unit for differentially amplifying signals inputted to an inverting input terminal and non-inverting input terminal to reduce an input offset voltage and outputting the amplified signal to an output terminal; and

a slew enhancing unit for increasing a slew rate of the amplified signal outputted to the output terminal on the basis of the input voltage value of the inverting input terminal and the input voltage value of the non-inverting input terminal.

2. The amplifier of claim 1, wherein the amplifying unit and the slew enhancing unit are implemented by a plurality of CMOS (Complementary Metal Oxide Semiconductor).

3. The amplifier of claim 1, wherein the amplifying unit comprises:

a first differential amplifier for differentially amplifying a signal inputted to the inverting input terminal and the non-inverting input terminal;

a symmetrical amplifier for generating a signal symmetrical to the signal outputted from the non-inverting output terminal of the first differential amplifier and differentially amplifying the generated signal and the signal outputted from the non-inverting output terminal of the first differential amplifier; and

an amplified signal output unit for differentially amplifying signals inputted from an inverting output terminal and a non-inverting output terminal of the symmetrical amplifier and outputting the amplified signals to the output terminal.

4. The amplifier of claim 3, wherein the amplifying unit further comprises:

a compensator for guaranteeing a frequency stability through a frequency compensation of the amplifier.

5. The amplifier of claim 4, wherein the compensator includes a resister and a condenser connected in series to the resister.

6. The amplifier of claim 3, wherein the symmetrical amplifier comprises:

an input symmetry unit for generating a signal symmetrical to the signal outputted from the non-inverting output terminal of the first differential amplifier and outputting the generated signal; and

a second differential amplifier for differentially amplifying the signal outputted from the non-inverting output terminal of the first differential amplifier and the signal generated by the input symmetry unit.

7. The amplifier of claim 6, wherein the input symmetry unit amplifies a common voltage of signals inputted to the inverting input terminal and the non-inverting input terminal and generates the symmetrical signal.

8. The amplifier of claim 3, wherein the slew enhancing unit comprises:

a discharge controller for generating a signal for discharging a current charged in a capacitive load connected to the output terminal on the basis of the

signal outputted from the non-inverting output terminal of the first differential amplifier and the signal generated by the symmetry amplifier;

a charge controller for generating a signal for charging a current to the capacitive load connected to the output terminal on the basis of the signal outputted from the inverting output terminal of the first differential amplifier; and

a discharge/charge driving unit for discharging a current charged in the capacitive load connected to the output terminal or charging a current to the capacitive load on the basis of the signals generated from the discharge controller and the charge controller.

9. The amplifier of claim 8, wherein when an input voltage value of the inverting input terminal is greater than an input voltage value of the non-inverting input terminal and a voltage difference between the inverting input terminal and the non-inverting input terminal is greater than a prescribed voltage, the discharge controller discharges a current charged in the capacitive load.

10. The amplifier of claim 9, wherein when the input voltage value of the inverting input terminal is greater than the input voltage value of the non-inverting input terminal and the voltage difference between the inverting input terminal and the non-inverting input terminal is smaller than a prescribed voltage, the discharge controller stops discharging of the current charged in the capacitive load.

11. The amplifier of claim 8, wherein when the input voltage value of the non-inverting input terminal is greater than the input voltage value of the

inverting input terminal and the voltage difference between the inverting input terminal and the non-inverting input terminal is greater than a prescribed voltage, the charge controller charges a current into the capacitive load.

12. The amplifier of claim 11, wherein when the input voltage value of the non-inverting input terminal is greater than the input voltage value of the inverting input terminal and the voltage difference between the inverting input terminal and the non-inverting input terminal is smaller than a prescribed voltage, the charge controller stops charging of the current into the capacitive load.

13. The amplifier of claim 11, wherein the capacitive load is each pixel of an LCD (Liquid Crystal Display) connected to the output terminal of the amplifying unit.